

Standard Test Method of Measurement of Common-Emitter DC Current Gain of Junction Transistors¹

This standard is issued under the fixed designation F 528; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This test method covers the measurement of common-emitter dc current gain (forward, h_{FE} , or inverted, h_{FEI}) of bipolar transistors, for which the collector-emitter leakage current, I_{CEO} , is less than 10 % of the collector current, I_C , at which the measurement is to be made, and for which the shunt leakage current in the base circuit is less than 10 % of the base current required.

1.2 This test method is suitable for measurement of common-emitter dc current gain at a single given value of test transistor collector current or over a given range of collector currents (for example, over the range of the transistor to be tested).

1.2.1 The nominal ranges of collector current over which the three test circuits are intended to be used are as follows:

- 1.2.1.1 *Circuit 1*, less than 100 μ A,
- 1.2.1.2 *Circuit 2*, from 100 μ A to 100 mA, and
- 1.2.1.3 *Circuit 3*, greater than 100 mA.

1.3 This test method incorporates tests to determine if the power dissipated in the transistor is low enough that the temperature of the junction is approximately the same as the ambient temperature.

1.4 The values stated in International System of Units (SI) are to be regarded as standard. No other units of measurement are included in this standard.

1.5 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Terminology

2.1 Definitions:

2.1.1 *common-emitter dc current gain, h_{FE}* —the ratio of dc collector current (in excess of collector-emitter leakage current I_{CEO}) to base current when the transistor is connected in the common-emitter configuration (see Fig. 1a); that is:

$$h_{FE} = (I_C - I_{CEO})/I_B$$

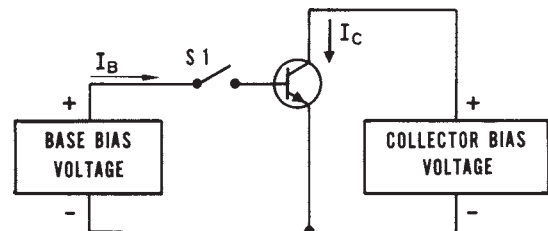
2.1.2 *inverted common-emitter dc current gain, h_{FEI}* —the ratio of dc emitter current I_E (in excess of emitter-collector leakage current I_{ECO}) to base current when the transistor is connected in the common-collector configuration (see Fig. 1b); that is:

$$h_{FEI} = (I_E - I_{ECO})/I_B$$

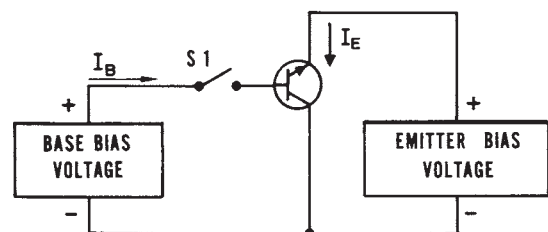
NOTE 1—In the remainder of this test method only h_{FE} is discussed. Measurements and calculations for h_{FEI} are identical and the same apparatus and procedures apply.

3. Summary of Test Method

3.1 Sufficient current, I_B , is driven into the base of a transistor to achieve the desired collector current at the required collector-emitter voltage. The magnitude of the base



(a) I_{CEO} IS THE COLLECTOR CURRENT WITH S 1 OPEN



(b) I_{ECO} IS THE EMITTER CURRENT WITH S 1 OPEN

NOTE 1—The transistor shown is an npn type; for pnp types the polarities of the bias supplies are reversed.

FIG. 1 Explanatory Circuits to Illustrate the Meaning of Terms Used in Calculation of h_{FE} and h_{FEI}

¹ This test method is under the jurisdiction of ASTM Committee F01 on Electronics, and is the direct responsibility of Subcommittee F01.11 on Quality and Hardness Assurance.

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