



Standard Practice for Determining Safe Current Pulse-Operating Regions for Metallization on Semiconductor Components (Metric)¹

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1. Scope

1.1 This practice covers procedures for determining operating regions that are safe from metallization burnout induced by current pulses of less than 1-s duration.

NOTE 1—In this practice, “metallization” refers to metallic layers on semiconductor components such as interconnect patterns on integrated circuits. The principles of the practice may, however, be extended to nearly any current-carrying path. The term “burnout” refers to either fusing or vaporization.

1.2 This practice is based on the application of unipolar rectangular current test pulses. An extrapolation technique is specified for mapping safe operating regions in the pulse-amplitude versus pulse-duration plane. A procedure is provided in [Appendix X2](#) to relate safe operating regions established from rectangular pulse data to safe operating regions for arbitrary pulse shapes.

1.3 This practice is not intended to apply to metallization damage mechanisms other than fusing or vaporization induced by current pulses and, in particular, is not intended to apply to long-term mechanisms, such as metal migration.

1.4 This practice is not intended to determine the nature of any defect causing failure.

1.5 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Terminology

2.1 Definitions of Terms Specific to This Standard:

2.1.1 *failure*—a change in the measured resistance of $\pm 10\% \Delta R/R$ or as agreed upon by the parties to the test.

3. Summary of Practice

3.1 Specimens are selected from the population being evaluated.

3.2 The d-c resistance of each specimen is measured.

3.3 Each specimen is subjected to stress from rectangular current pulses varying in amplitude and duration according to a predetermined schedule of pulse width and amplitudes.

3.4 A second d-c resistance measurement is made on each specimen after each pulse, and it is characterized as having failed or survived.

3.5 The number, x , of specimens surviving and the total number, n , of specimens tested at each pulse width and amplitude are analyzed statistically to determine the burnout level at each test pulse width for the desired burnout survival probability and confidence level.

3.6 A point corresponding to the burnout level (at the desired probability and confidence level) is plotted for each of the test pulse duration values in the pulse-amplitude, pulse-duration plane. Based on these points, an extrapolation technique is used to plot the boundary of the safe operating region.

3.7 The following items are not specified by the practice and are subject to agreement by the parties to the test:

3.7.1 The procedure by which the specimens are to be selected.

3.7.2 Test patterns that will be representative of adjacent metallization on a die or wafer ([5.3](#)).

3.7.3 The schedule of pulse amplitudes and durations to be applied to the test samples ([9.8](#)).

3.7.4 The level of probability and confidence to be used in calculations to establish the boundary of the safe operating region ([10.1](#)).

3.7.5 The amount of change of resistance that will define the criterion for failure.

3.7.6 The statistical model to be used to determine the burnout probability at a desired stress level.

3.7.7 The form and content of the report.

4. Significance and Use

4.1 Solid-state electronic devices subjected to stresses from excessive current pulses sometimes fail because a portion of the metallization fuses or vaporizes (suffers burnout). Burnout susceptibility can vary significantly from component to component on a given wafer, regardless of design. This practice

¹ This practice is under the jurisdiction of ASTM Committee F01 on Electronics and is the direct responsibility of Subcommittee F01.11 on Nuclear and Space Radiation Effects.

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