



Standard Specification for Format, Physical Properties, and Test Methods for 19 and 35 mm Testable Tape Carrier for Perimeter Tape Carrier- Bonded Semiconductor Devices¹

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INTRODUCTION

It is the purpose of this specification to facilitate interchangeability of carrier tape produced by various manufacturers. Standardization is also intended to promote efficient utilization of equipment used to test devices on tape and assemble them to hybrid circuits. A complete description of a particular carrier tape requires specification of a considerable number of parameters not covered by this standard. This standard specification includes only elements of format design for which substantial consensus with respect to technically and economically sound commercial practice has been achieved.

1. Scope

1.1 This specification covers standard formats for testable semiconductor lead carrier tape suitable for hybrid applications.

1.2 This standard specifies tape width, configuration, and location of guide perforations (“sprocket holes”), location of lead pattern frames on tape, lead pattern window size, and placement of outer lead bond and electrical test pad areas in the lead pattern.

1.3 The values stated in inch-pound units are to be regarded as the standard. The values given in parentheses are for information only.

1.4 The following hazard caveat pertains only to the test method portion, Section 7 of this specification. *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Terminology

2.1 Definitions:

2.1.1 *lead pattern window*—in tape carrier bonding, the area in each frame in which plastic backing of plastic/metal composite tape is totally or partially removed to expose appropriate areas of bare conducting leads for attachment to a

microelectronic device on the inner end and a mounting substrate on the outer end.

2.1.2 *outer lead bond area*—in tape carrier bonding, that area on each lead which will be connected to a mounting substrate.

2.1.3 *tape format*—in tape carrier bonding, the layout design elements of carrier tape, including the topographical arrangement of lead pattern elements and test contacts in each frame, description of the placement of frames upon the tape, and the specification of tape width and the placement of mechanical handling aids, such as guide perforations.

2.1.4 *testable tape carrier*—in microelectronic fabrication, a continuous length of plastic/metal composite film, superficially resembling motion picture film, which carries at each frame position a repetitive pattern of electrically conducting leads and test contacts.

2.1.4.1 *Discussion*—The lead arrangement is designed so as to electrically interconnect points on a microelectronic device with contacts on the mounting substrate of the device. The test contacts permit static or dynamic evaluation, or both, of each microelectronic device prior to assembly to a mounting substrate.

2.1.5 *test pads*—in tape carrier bonding, conducting areas in each tape frame position that can be contacted electrically by probes in order to test devices attached to the tape.

3. Classification

3.1 A wide variety of formats are covered under this standard. Tape format style is classified according to the following code:

“Style A–B–C–D–E–F–G–H–I–J”

¹ This specification is under the jurisdiction of ASTM Committee F01 on Electronics and is the direct responsibility of Subcommittee F01.07 on Wire Bonding, Flip Chip, and Tape Automated Bonding.

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