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AMERICAN SOCIETY FOR TESTING AND MATERIALS
100 Barr Harbor Dr., West Conshohocken, PA 19428
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Standard Test Method for Measuring Resistivity Profiles Perpendicular to the Surface of a Silicon Wafer Using a Spreading Resistance Probe [1]

This standard is issued under the fixed designation F 672; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ϵ) indicates an editorial change since the last revision or reapproval.

ϵ^1 NOTE—Keywords were added editorially in January 1995.

INTRODUCTION

The measurement of resistivity profile by means of a spreading resistance probe is a complex procedure, with a number of commonly accepted options for carrying out the component measurements. ASTM Committee F-1 on Electronics has designed this test method to allow a range of choices, consistent with good practice, for the electronic configuration, type of specimen preparation, and method for measuring bevel angle. Items not specified by this test method are to be agreed upon by the parties to the test, usually from a specified set of choices in the context of a general restriction. The measurement of bevel angle is particularly difficult to specify, as the selection of an appropriate method depends not only on the range of angle measured but also on the quality of the instrumentation available for that method. Although ideally the beveled surface and the original surface should be two planes intersecting along a straight line, the actual geometry may differ from this ideal, further complicating the measurement. These points are recognized in the section on interferences and in Appendix X1 and associated references on the bevel-angle measurement.

1. Scope

1.1 This test method covers measurement of the resistivity profile perpendicular to the surface of a silicon wafer of known orientation and type.

NOTE 1—This test method may also be applicable to other semiconductor materials, but feasibility and precision have been evaluated only for silicon and germanium.

1.2 This test method may be used on epitaxial films, substrates, diffused layers, or ion-implanted layers, or any combination of these.

1.3 This test method is comparative in that the resistivity profile of an unknown specimen is determined by comparing its measured spreading resistance value with those of calibration standards of known resistivity. These calibration standards must have the same surface preparation, conductivity type, and crystallographic orientation as the unknown specimen.

1.4 This test method is intended for use on silicon wafers in any resistivity range for which there exist suitable standards. Polished, lapped, or ground surfaces may be used.

1.5 This test method is destructive in that the specimen must be beveled.

1.6 Correction factors, which take into account the effects of boundaries or local resistivity variations with depth, are needed prior to using calibration data to calculate resistivity from the spreading resistance values.

NOTE 2—This test method extends Method F 525 to depth profiling.

NOTE 3—This test method provides means for directly determining the resistivity profile of a silicon specimen normal to the specimen surface. Unlike Method F 84 and Test Methods F 374 and F 419, it can provide lateral spatial resolution of resistivity on the order of a few micrometres, and an in-depth spatial resolution on the order of 10 nm (100 Å). This test method can be used to profile through *p-n* junctions.

1.7 This test method is primarily a measurement for determining the resistivity profile in a silicon wafer. However, common practice is to convert the resistivity profile information to a density profile. For such purposes, a conversion between resistivity and majority carrier density is provided in Appendix X2.

1.8 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.* Specific hazard statements are given in Section 9.

2. Referenced Documents

2.1 *ASTM Standards:*

[1] This test method is under the jurisdiction of ASTM Committee F-1 on Electronicsand is the direct responsibility of Subcommittee F01.06 on Silicon Material and Process Control.

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