



Designation: F 928 – 93 (Reapproved 1999)

Standard Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates¹

This standard is issued under the fixed designation F 928; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 These test methods² provide means for examining the edge contour of circular wafers of silicon, gallium arsenide, and other electronic materials, and determining fit to limits of contour specified by a template that defines a permitted zone through which the contour must pass. Principal application of such a template is intended for, but not limited to, wafers that have been deliberately edge shaped.

1.2 Two test methods are described. One is destructive and is limited to inspection of discrete points on the periphery, including flats. The contour of deliberately edge-shaped wafers may not be uniform around the entire periphery, and thus the discrete location(s) may or may not be representative of the entire periphery. The other test method is nondestructive and suitable for inspection of all points on the wafers periphery except flats.

1.3 The nondestructive test method may also be applied to the examination of the edge contour of the outer periphery of substrates for rigid disks used for magnetic storage of data.

NOTE 1—Reference to wafers in the remainder of this standard shall be interpreted to include substrates for rigid disks unless the phrase “of electronic materials” is also included in the context.

1.4 The values stated in SI units are to be regarded as the standard. The values given in parentheses are for information only.

1.5 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Referenced Documents

2.1 ASTM Standards:

E 122 Practice for Choice of Sample Size to Estimate a

¹ These test methods are under the jurisdiction of ASTM Committee F-1 on Electronics and are the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

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² DIN 50441/2 is equivalent to Method B of this standard. It is the responsibility of DIN Committee NMP 221 with which Committee F-1 maintains close technical liaison. DIN 50441/2, Measurement of the Geometric Dimensions of Semiconductor Slices; Testing of Edge Rounding, is available from Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-1000 Berlin 30, FRG.

Measure of Quality for a Lot or Process³

2.2 Military Standard:

MIL-STD-105D Sampling Procedures and Tables for Inspection by Attributes⁴

2.3 SEMI Standards:

SEMI M1, Specifications for Polished Monocrystalline Silicon Wafers⁵

SEMI M9, Specifications for Polished Monocrystalline Gallium Arsenide Slices⁵

3. Summary of Test Methods

3.1 Both test methods employ optical means to project a shadow of the edge contour at substantial magnification on a screen. In applying Method A (destructive) the sample wafer is cleaved or broken along a diameter. A sharply focused image of the cross section of the wafer is obtained over a sufficiently large region near the edge with the aid of an optical comparator or projection microscope. In Method B (nondestructive) the unbroken wafer is back lighted with collimated (parallel) light such that a sharply defined shadow of the wafer edge is projected on a screen. In this test method the wafer is not altered in any way.

3.2 By either test method, the contour of the wafer edge profile image is compared to a template that has been mounted or projected on the screen. The template defines a permitted zone through which the edge contour must pass.

4. Significance and Use

4.1 The edges of circular wafers of electronic materials are frequently required to be shaped after cutting the wafers from the ingot. Contouring the wafer edge reduces the incidence of chipping and minimizes epitaxial edge crown and photoresist edge bead during subsequent processing of the wafer. Similarly, edges of rigid disk substrates are frequently edge shaped.

4.2 The test methods described here provide means to determine that the wafer edge contour is appropriate to meet specifications, such as SEMI M1 or SEMI M9, which are intended to provide wafers avoiding the difficulties enumerated above.

³ *Annual Book of ASTM Standards*, Vol 14.02.

⁴ Available from Standardization Documents Order Desk, Bldg. 4 Section D, 700 Robbins Ave., Philadelphia, PA 19111-5094, Attn: NPODS.

⁵ Available from the Semiconductor Equipment and Materials International, 805 East Middlefield Road, Mountain View, CA 94043.