



Standard Practice for Shallow Etch Pit Detection on Silicon Wafers¹

This standard is issued under the fixed designation F 1049; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This practice is used to detect shallow etch pits, which may be related to the level of metallic impurities near the surface of silicon epitaxial or polished wafers.

1.2 This practice is not recommended for use in defect density evaluations, but as a subjective means of estimating defect densities and distributions on the surface of a polished or epitaxial wafer.

1.3 Silicon crystals doped either *p*- or *n*-type and with resistivities as low as 0.005 Ω·cm may be evaluated. This practice is applicable for silicon wafers grown in either a (111) or (100) crystal orientation.

1.4 This practice utilizes a thermal oxidation process followed by a chemical preferential etchant to create and then delineate shallow etch pits.

1.5 The values stated in acceptable metric units are to be regarded as the standard. The values in parentheses are for information only.

1.6 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.* Specific hazard statements are given in Section 9.

2. Referenced Documents

2.1 ASTM Standards:

D 5127 Guide for Electronic Grade Water²

F 154 Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces³

F 1725 Guide for Analysis of Crystallographic Perfection of Silicon Ingots³

F 1727 Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers³

F 1809 Guide for Selection and Use of Etching Solutions to Delineate Structural Defects in Silicon³

F 1810 Test Method for Counting Preferentially Etched or Decorated Surface Defects in Silicon Wafers³

2.2 SEMI Standards:

SEMI C 1 Specifications for Reagents⁴

M 17 Specification for a Universal Wafer Grid⁴

3. Terminology

3.1 Definitions:

3.1.1 *haze*—on a semiconductor wafer, non—localized light scattering resulting from surface topography (microroughness) or from dense concentrations of surface or near-surface imperfections. See also **laser light scattering event**.

3.1.1.1 *Discussion*—Haze due to the existence of a collection of imperfections of the type that result in haze cannot be readily distinguished by the eye or other optical detection system without magnification. In a scanning surface inspection system, haze and laser-light scattering events comprise the laser surface scanner signal due to light scattering from a wafer surface.

3.1.2 *shallow etch pits*—etch pits that are small and shallow in depth under high magnification, > 200×.

3.1.2.1 *Discussion*—Shallow etch pits on silicon wafers are shown in Guide F 154.

3.1.3 *saucer pits*—same as **shallow etch pits**, see 3.1.2.

4. Summary of Practice

4.1 Silicon wafers, either epitaxial or polished, are thermally oxidized and preferential etched. This will reveal small etch pits, shallow in depth, when observed through an interference contrast microscope. The distribution of the etch pits on the surface of the wafer are determined by illuminating the wafer with a high intensity lamp.

5. Significance and Use

5.1 High levels of etch pits are reported⁵ to indicate metallic contamination that is detrimental to wafer processing. This can be deduced from the density of etch pits on the surface of the wafer.

5.2 This practice is appropriate for process control, and research and development applications. Because its reproducibility has not been established by interlaboratory test, it is not recommended for use in materials acceptance unless the parties

¹ This practice is under the jurisdiction of ASTM Committee F-1 on Electronics and is the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

Current edition approved June 10, 2000. Published August 2000. Originally published as F 1049 – 87. Last previous edition F 1049 – 95.

² Annual Book of ASTM Standards, Vol 11.01.

³ Annual Book of ASTM Standards, Vol 10.05.

⁴ Available from Semiconductor Equipment and Materials International, 805 E. Middlefield Rd., Mountain View, CA 94043.

⁵ Pearce, C. W., and McMahon, R. G., "Role of Metallic Contamination in the Formation of 'Saucer' Pit Defects in Epitaxial Silicon," *Journal of Vacuum Science and Technology*, Vol 14, No. 1, 1977, p. 40.