



Standard Test Method for Estimating Electromigration Median Time-To-Failure and Sigma of Integrated Circuit Metallizations [Metric]¹

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1. Scope

1.1 This test method is designed to characterize the failure distribution of interconnect metallizations such as are used in microelectronic circuits and devices that fail due to electromigration under specified d-c current density and temperature stress. This test method is intended to be used only when the failure distribution can be described by a log-Normal distribution.

1.2 This test method is intended for use as a referee method between laboratories and for comparing metallization alloys and metallizations prepared in different ways. It is not intended for qualifying vendors or for determining the use-life of a metallization.

1.3 The test method is an accelerated stress test of four-terminal structures (see Guide F 1259M) where the failure criterion is either an open circuit in the test line or a prescribed percent increase in the resistance of the test structure.

1.4 This test method allows the test structures of a test chip to be stressed while still part of the wafer (or a portion thereof) or while bonded to a package and electrically accessible by means of package terminals.

1.5 This test method is not designed to characterize the metallization for failure modes involving short circuits between adjacent metallization lines or between two levels of metallization.

1.6 This test method is not intended for the case where the stress test is terminated before all parts have failed.

1.7 This test method is primarily designed to analyze complete data. An option is provided for analyzing censored data (that is, when the stress test is halted before all parts under test have failed).

1.8 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appro-*

priate safety and health practices and determine the applicability of regulatory limitations prior to use.

2. Referenced Documents

2.1 ASTM Standards:

F 1259M Guide for Design of Flat, Straight-Line Test Structures for Detecting Metallization Open-Circuit or Resistance-Increase Failure due to Electromigration [Metric]²

F 1261M Test Method for Determining the Average Electrical Width of a Straight, Thin-Film Metal Line [Metric]²

2.2 Other Standards:

EIA/JEDEC Standard 33-A— Standard Method for Measuring and Using the Temperature Coefficient of Resistance to Determine the Temperature of a Metallization Line³

EIA/JEDEC Standard 37— Lognormal Analysis of Uncensored Data, and of Singly Right-Censored Data Utilizing the Persson and Rootzen Method³

3. Terminology

3.1 Definitions of Terms Specific to This Standard:

3.1.1 *metallization*—the thin-film metallic conductor used as electrical interconnects in a microelectronic integrated circuit.

3.1.2 *test chip*—an area on a wafer containing one or more test structures that are stressed according to the test method while either is still part of the wafer or after having been separated and packaged.

3.1.3 *test line*—a straight metallization line of designed uniform width that is subjected to the current density and temperature stresses prescribed in the test method.

3.1.4 *test structure*—a passive metallization structure, with terminals to permit electrical access, that is fabricated on a semiconductor wafer by the normal procedures used to manufacture microelectronic integrated devices.

¹ This test method is under the jurisdiction of ASTM Committee F01 on Electronics and is the direct responsibility of Subcommittee F01.11 on Quality and Hardness Assurance.

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² *Annual Book of ASTM Standards*, Vol 10.04.

³ Available from Global Engineering, 15 Inverness Way, East Englewood, CO 80112-5776.