



Designation: F 1393 – 92 (Reapproved 1997)

AMERICAN SOCIETY FOR TESTING AND MATERIALS
100 Barr Harbor Dr., West Conshohocken, PA 19428
Reprinted from the Annual Book of ASTM Standards. Copyright ASTM

Standard Test Method for Determining Net Carrier Density in Silicon Wafers by Miller Feedback Profiler Measurements With a Mercury Probe¹

This standard is issued under the fixed designation F 1393; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This test method² covers the measurement of net carrier density and net carrier density profiles in epitaxial and polished bulk silicon wafers in the range from about 4×10^{13} to about 8×10^{16} carriers/cm (resistivity range from about 0.1 to about 100 Ω -cm in *n*-type wafers and from about 0.24 to about 330 Ω -cm in *p*-type wafers).

1.2 This test method requires the formation of a Schottky barrier diode with a mercury probe contact to an epitaxial or polished wafer surface. Chemical treatment of the silicon surface may be required to produce a reliable Schottky barrier diode. (1)³ The surface treatment chemistries are different for *n*- and *p*-type wafers. This test method is sometimes considered destructive due to the possibility of contamination from the Schottky contact formed on the wafer surface; however, repetitive measurements may be made on the same test specimen.

1.3 This test method may be applied to epitaxial layers on the same or opposite conductivity type substrate. This test method includes descriptions of fixtures for measuring substrates with or without an insulating backseal layer.

1.4 The depth of the region that can be profiled depends on the doping level in the test specimen. Based on data reported by Severin (1) and Grove (2), Fig. 1 shows the relationship between depletion depth, dopant density, and applied voltage together with the breakdown voltage of a mercury silicon contact. The test specimen can be profiled from approximately the depletion depth corresponding to an applied voltage of 1 V to the depletion depth corresponding to the maximum applied voltage (200 V or about 80 % of the breakdown voltage, whichever is lower). To be measured by this test method, a layer must be thicker than the depletion depth corresponding to an applied voltage of 2 V.

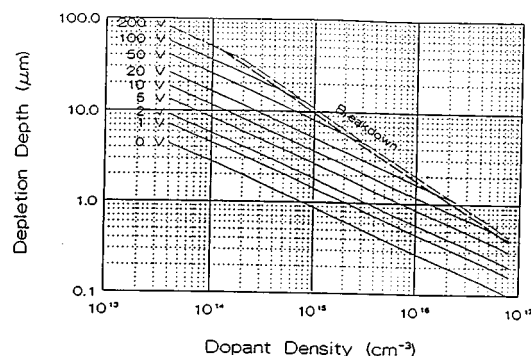
1.5 This test method is intended for rapid carrier density

¹ This test method is under the jurisdiction of ASTM Committee F-1 on Electronics and its the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

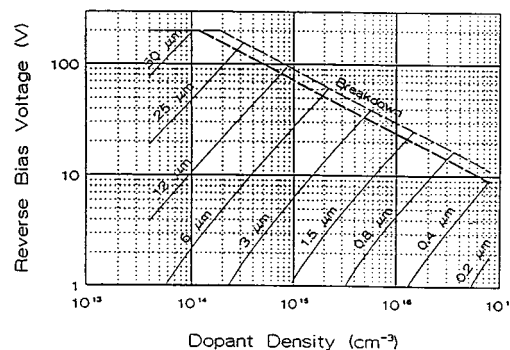
Current edition approved May 15, 1992. Published July 1992.

² DIN 50439, Determination of the Dopant Concentration Profile of a Single Crystal Semiconductor Material by Means of the Capacitance-Voltage Method and Mercury Contact, is the responsibility of DIN Committee NMP 221, with which Committee F-1 maintains close liaison. DIN 50439 is available from Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-1000, Berlin 30, Germany.

³ The boldface numbers in parenthesis refer to the list of references at the end of this test method.



(a) Depletion Depth as a Function of Dopant Density with Applied Reverse Bias Voltage as a Parameter.



(b) Applied Reverse Bias Voltage as a Function of Dopant Density with Depletion Depth as a Parameter.

NOTE 1—The light dashed line represents the applied reverse bias voltage at which breakdown occurs in a mercury silicon contact; the heavy dashed line represents 80 % of this voltage, it is recommended that the applied reverse bias voltage not exceed this value. The light chain-dot line represents the maximum reverse bias voltage specified in this test method.

FIG. 1 Relationships between Depletion Depth, Applied Reverse Bias Voltage, and Dopant Density

determination when extended sample preparation time or high temperature processing of the wafer is not practical.

NOTE 1—Test Method F 419 is an alternative method for determining net carrier density profiles in silicon wafers from capacitance-voltage measurements. This test method requires the use of one of the following structures: (1) a gated or ungated *p-n* junction diode fabricated using either planar or mesa technology or (2) an evaporated metal Schottky diode. Although this test method was written prior to consideration of the Miller Feedback Method, the Miller Feedback Method has been satisfactorily used in measuring the round robin samples.

1.6 This test method provides for determining the effective