

Standard Guide for Selection and Use of Etching Solutions to Delineate Structural Defects in Silicon¹

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1. Scope

1.1 This guide covers the formulation, selection, and use of chemical solutions developed to reveal structural defects in silicon wafers. Etching solutions identify crystal defects that adversely affect the circuit performance and yield of silicon devices. Sample preparation, temperature control, etching technique, and choice of etchant are all key factors in the successful use of an etching method. This guide provides information for several etching solution and allows the user to select according to the need. For further information see Appendix X1 and Figs. 1-32. For a test method for counting preferentially etched or decorated surface defects in silicon wafers see Test Method F 1810.

1.2 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Referenced Documents

2.1 ASTM Standards:

D 5127 Practice for Electronic Grade Water²

F 1725 Guide for Analysis of Crystallographic Perfection in Silicon Ingots³

F 1726 Guide for Analysis of Crystallographic Perfection in Silicon Wafers³

F 1727 Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers³

F 1810 Method for Counting Preferentially Etched or Decorated Surface Defects in Silicon Wafers³

2.2 SEMI Specifications:

SEMI C-1 Specification for Reagents⁴

3. Significance and Use

3.1 Structural defects formed in the bulk of a silicon wafer

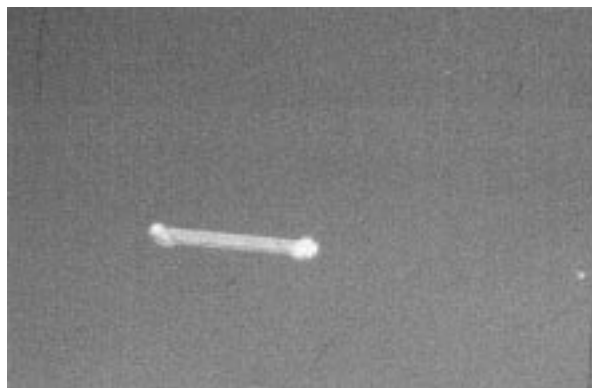


FIG. 1 Secco Etch With Agitation, Oxidation Stacking Fault, 1000x, [100], (1100°C Steam, 80 minutes), ~4 μm removal.

during its growth or induced by electronic device processing can affect the performance of the circuitry fabricated on that wafer. These defects take the form of dislocations, slip, stacking faults, shallow pits, or precipitates.

3.2 The exposure of the various defects found on or in a silicon wafer is often the first critical step in evaluating wafer quality or initiating failure analysis of an errant device structure. Etching often accomplishes this task.

4. Interferences

4.1 Complicating factors are different for each etchant. Research the choice of etchants in advance to ensure the

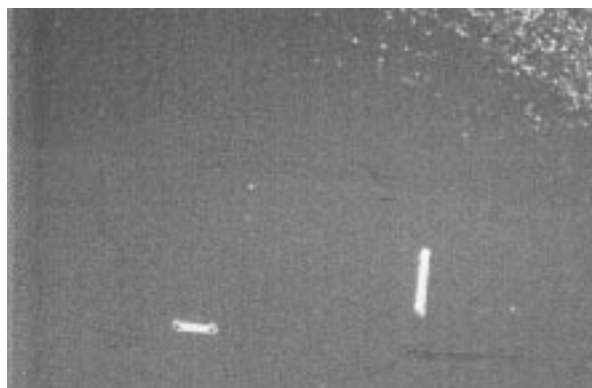


FIG. 2 Secco Etch With Agitation, Oxidation Stacking Fault, 400x, [100], (1100°C Steam, 80 minutes), ~4 μm removal.

¹ This guide is under the jurisdiction of ASTM Committee F01 on Electronics and is the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

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² Annual Book of ASTM Standards, 11.01

³ Annual Book of ASTM Standards, Vol 10.05.

⁴ Available from Semiconductor Equipment and Materials International, 805 E. Middlefield Rd., Mountain View, CA 94043.